claims 12, 13 and 14, and the specification. Accordingly, no new matter has been entered.

Objection to Claims 3 and 10

Claims 3 and 10 are objected to for the noted informalities in the official action. The objected claims are accordingly amended by the above claim amendments, which are unrelated to patentability issues.

Claim Rejections - 35 USC § 103

The Examiner rejected claims 1-9 and 11-14 under 35 USC § 103(a) as being unpatentable over Pan (US 5,750,435). Additionally, claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pan in view of the admitted prior art. Furthermore, claims 12-14 are rejected as unpatentable over Pan in view of Motoyoshi et al. (JP 6-53492).

Pan teaches the presence of hardening ions 18 which are implanted into the gate oxide 14 regions of a FET device beneath both edges of the gate electrode 16. Pan states that the implanting of the hardening ions 18 into the gate oxide 14 beneath both edges of the gate electrode 16 is critical to his invention. Pan also discloses that in addition to implanting hardening ions 18 into the gate oxide 14 regions beneath both edges of the gate electrode 16, hardening ions are further provided during the implantation step to the exposed surfaces of the gate electrode16, the exposed surfaces of the gate oxide, and the upper surface of the semiconductor substrate 10. See column 5, line 60 - column 6, line 5. Pan further discloses an ion implant dose of about 1E14 to about 1E16 ion per square centimeter, see column 6, lines 6-21. Therefore, except for the unhardened portion of the gate oxide directly underneath and inwards of the gate electrode edges, the ion concentration in the remaining hardened portions of the oxide is substantially the same. Accordingly, Pan does not disclose, teach, or suggest, explicitly nor impliedly, a circuit structure having a portion of the gate oxide layer underneath the gate electrode having an ion implant concentration higher than adjacent/remaining portions of the oxide layer as is recited in amended independent claims 1, 3, 12, and new claim 45.

Motoyoshi et al. discloses uniform orthogonal fluorine implanting over the entire surface of gate oxide. Accordingly, Motoyoshi et al. also fail to disclose, teach, or suggest, explicitly or impliedly, a circuit structure having a portion of the gate oxide layer underneath the gate electrode having an ion implant concentration higher than adjacent/remaining portions of the oxide layer. Accordingly, one skilled in the art combining the teachings of Motoyoshi et al. with Pan would fail to produce the claimed invention recited in amended independent claims 1, 3, 12, and new claim 45. Accordingly, Applicants assert that claims 1,3, 12 and 45, and the claims that depend therefrom, are patentable over the cited prior art and, therefore, respectfully requests that the obviousness rejections to the claims be withdrawn.

CONCLUSION

The Applicant respectfully submits that, in view of the above amendments and remarks, the application is now in condition for allowance. The Examiner is encouraged to contact the undersigned to resolve efficiently any formal matters or to discuss any aspects of the application or of this response. Otherwise, early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,

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Appendix A

Version indicating changes made, additions underscored, deletions stricken.

Please replace the paragraph on page 6, lines7-9, with the following:

--FIGS. 3a through 3d~~3e~~, schematically illustrate a series of cross-sectional representations which illustrate the progressive stages in completing the fabrication of a FET device in accordance with a process of the present invention.--

Please replace the paragraph on page 8, starting at line 4 with the following revised paragraph:

--Generally, although not necessary for the practice of~~if~~ the invention, further materials may be deposited to form additional material layers upon the polysilicon layer 18 of the gate electrode 16. The typical materials~~material~~ of these layers include metals, metal alloys, highly doped polysilicon, silicides, and polycides (polysilicon/metal silicide stacks), which are used with the purpose to improve the electrical characteristics of the device. In a preferred embodiment, a relatively thin layer of titanium nitride (TiN) is deposited on the polysilicon layer 18 to form a barrier layer 20. The barrier layer 20 is then blanketed with a tungsten (W) layer 22 to complete the formation of the gate electrode 16.--

Please replace the paragraph on page 12, starting at line 2 with the following revised paragraph:

--In forming the source/drain regions 28a and 28b, a first ion implantation is made using the gate electrode 16 and the field isolation regions 12 to mask the substrate, in order to form the more lightly doped portions of LDD source/drain regions 30a and 30b. Generally, although not necessary for the practice if the invention, as shown by FIG. 3c, provided on both sides of the gate electrode 16 are electrode spacers 32. The electrode spacers 32 may be formed from materials including but not limited to insulating materials

such as silicon oxides, silicon nitrides and silicon oxynitrides. Various processes are used to form electrode spacers 32. Such processes include Reactive Ion Etch (RIE), and the above mentioned material deposition methods. Typically, electrode spacers 32 are formed by depositing an oxide film, such as tetraethoxysilane (TEOS) oxide at between about 600 to about 720 degrees centigrade to a thickness of between about 300 Å to about 700 Å. A second ion implantation is performed to complete the source/drain regions 28a and 28b with HDD source/drain regions 34a and 34b. In the illustrated FET device 2, the source/drain regions 28a and 28b~~20~~ may be doped with any n-type or p-type dopant or combinations of different n-type dopants or p-type dopants might be used to achieve different diffusion profiles. Further, it is to be appreciated that the angled ion implantation step of the present invention, if desired, could be carried out at this stage in the fabrication of the FET device 2, as there are no apparent advantages or disadvantage in performing this step before or after the formation of either the LDD, the spacers, or even the HDD.--

Please insert the following paragraph on page 15, between lines 7 and 8:

--For example, FIG. 3E illustrates a circuit structure comprising a semiconductor layer 10 and a first dopant-type MOS transistor 2a situated on the semiconductor layer 10 having a source region 28a and a drain region 28b in the semiconductor layer 10 which are doped with a first conductivity-type dopant 37a, a channel region 29 located between the source/drain regions 28a and 28b, a gate oxide layer 14a located on a surface of the channel region 29, and a gate electrode 16a located on the gate oxide layer 14a. The portion of the gate oxide layer 14a, which is beneath the gate electrode 16a and adjacent the drain region 28b and which defines an overlap region 26a, has an ion implant concentration which is effective to lower the surface electrical field in the overlap region 26a. A second-type dopant MOS transistor 2b, which is complementary to the first dopant-type MOS transistor 2a, is situated on the semiconductor layer 10 and includes a second gate oxide layer 14b, two complementary source/drain regions 28c and 28d, which are doped with a second conductivity-type dopant 37b, and a complementary gate electrode 16b located on the second gate oxide layer 14b. Additionally, a portion of the

second gate oxide layer 14b, which is beneath the complimentary gate electrode 16b and adjacent the complimentary drain region 28d and which defines a second overlap region 26b, has an ion implant concentration which is effective to lower the surface electrical field in the second overlap region 26b. Preferably, the ion implant concentration is about 1E18 atoms per cubic centimeter of fluorine.--

Please replace the Abstract, with the following amended abstract:

--~~A process for the fabrication of an~~An integrated circuit which provides a FET device having reduced GIDL current is described. A semiconductor substrate is provided wherein active regions are separated by an isolation region~~,~~ and a gate oxide layer is provided~~form~~ on the active regions. A gate electrode is provided~~Gate electrodes are formed~~ upon the gate oxide layer wherein ~~in the active regions. An angled, high dose, ion implant is performed to selectively dope the gate oxide layer~~ beneath an edge of ~~each~~ the gate electrode~~, in~~ a gate-drain overlap region having ~~,~~a high dose ion implant is provided. ~~and the fabrication of the integrated circuit is completed~~.--

In the claims

1. (Amended) A circuit structure comprising:

a semiconductor layer;

an oxide layer formed on said semiconductor layer;

~~a polysilicon layer formed on said oxide layer;~~

a gate structure formed on said oxide layer~~from said polysilicon layer, said gate structure~~ having a defined leading edge; and

an overlap region beneath said gate structure and adjacent said leading edge having a predetermined ion implant concentration higher than adjacent oxide layer portions, said predetermined implant concentration being sufficient to increase the electrical gate oxide thickness in said overlap region.

3. (Amended) A circuit structure comprising:

a semiconductor layer;

a source region and a drain region in said semiconductor layer which are lightly doped with a first conductivity-type dopant;

a channel region located between said source/drain regions;

a gate oxide layer located on a surface of said channel region; and

a gate electrode located on said gate oxide layer, a~~the~~ portion of said gate oxide layer, which is beneath said gate electrode and adjacent said drain region~~,~~ and which defines an overlap region, having an ion implant concentration higher than remaining portions of said oxide layer which is effective to lower the surface electrical field in said overlap region.

10. (Amended) The circuit structure according to claim 3, wherein said gate electrode is comprised of a layer of polysilicon, a layer of titanium nitride deposited on said polysilicon layer, and a layer of tungsten deposited on said titanium nitride layer.

12. (Amended) A circuit structure comprising:

a semiconductor layer;

a first dopant-type MOS transistor is situated on said semiconductor layer having:

a source region and a drain region in said semiconductor layer which are doped with a first conductivity-type dopant;

a channel region located between said source/drain regions;

a gate oxide layer located on a surface of said channel region; and

a gate electrode located on said gate oxide layer, a~~the~~ portion of said gate oxide layer, which is beneath said gate electrode and adjacent said drain region~~,~~ and which defines an overlap region, having an ion implant concentration higher than remaining portions of said gate oxide layer which is effective to lower the surface electrical field in said overlap region; and,

a second-type dopant MOS transistor which is complementary to said first dopant-type MOS transistor, said second-type dopant MOS transistor is situated on said semiconductor layer and includes a second gate oxide layer, two complementary source/drain regions which are doped with a second conductivity-type dopant, and a complementary gate electrode located on said second gate oxide layer.

14. (Amended) The circuit structure according to claim 12, wherein a~~the~~ portion of said second gate oxide layer which is beneath said complimentary gate electrode and adjacent said complimentary drain region, and which defines a second overlap region, having an ion implant concentration which is effective to lower the surface electrical field in said second overlap region.